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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NANO, SARGON N	
ART UNIT	PAPER NUMBER
2157	

DATE MAILED: 06/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/996,490	COGNET ET AL.	
	Examiner	Art Unit	
	Sargon N. Nano	2157	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is a response to application filed on Nov. 28 , 2001. Claims 1 – 30 are pending examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 – 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Pruthi U.S.Pub. No. 2004/0015582 9referred to hereafter as Pruthi)

Pruthi teaches a data communications , and in particular to a system and method for collecting , analyzing and monitoring data communications.

As to claim 1, Pruthi teaches a method for creating accurate time-stamped frames sent between computers via a network, comprising the steps of:

generating a time reference signal (see paragraph [0084 – 0085] Pruthi discloses the generation and reference signal packets);

synchronizing clocks associated with sending and receiving computers with the time reference signal(see paragraph [0084 – 0085] Pruthi discloses the synchronization of host and the interface clocks);

creating a test frame including a tag having reserved fields for transmit and receive time stamps(see paragraph [0074 – 0078] and [0081 – 0082] Pruthi discloses the time stamped on a packet at two separate network monitors);

inserting a transmit time stamp into the reserved transmit time stamp field corresponding to the time on the synchronized clock of the sending computer at the instant the test frame is sent onto the network (see paragraph [0074 – 0078] Pruthi discloses each packet is stamped at the sending and receiving nodes); and

receiving the test frame having the transmit time stamp and inserting a receive time stamp into the reserved receive time stamp field corresponding to the time on the synchronized clock of the receiving computer when the test frame was received by the receiving computer(see paragraph [0074 – 0078] Pruthi discloses each packet is stamped at the sending and receiving nodes).

As to claim 2, Pruthi teaches the method of claim 1, wherein the time reference signal is generated by a receiver for receiving a universal coordinated time signal (see paragraph [0081 – 0084]).

As to claim 3, Pruthi teaches the method of claim 2, wherein the universal coordinated time signal is received via a global positioning system receiver in

communication with either the sending or receiving computer (see paragraph [0081 – 0084]).

As to claim 4, Pruthi teaches the method of claim 3, wherein the clock and global positioning system receivers are electronically connected on a device which is attachable to an existing multi-master bus of either the sending or receiving computer (see paragraph [0081 – 0084]).

As to claim 5, Pruthi teaches the method of claim 4, wherein the device comprises a card interfacing with a multi-master bus of the receiving or sending computer (see paragraph [0081 – 0085] and [0143 – 0144]).

As to claim 6, Pruthi teaches the method of claim 2, wherein the synchronizing step includes the step of initializing the clocks with the received universal coordinated time signal and over time tracking and averaging the periodically received universal coordinated time signal and adjusting the clock to correspond to the universal coordinated time signal (see paragraph [0081 – 0085]).

As to claim 7, Pruthi teaches the method of claim 6, wherein the synchronizing step includes the steps of altering the voltage applied to a voltage controlled crystal oscillator associated with the clock to maintain synchronization with the universal coordinated time signal (see paragraph [0081 – 0085]).

As to claim 8, Pruthi teaches the method of claim 1, wherein the clock operates independent of an operating system clock within the sending or receiving computer(see paragraph [0081 – 0085]).

As to claim 9, Pruthi teaches the method of claim 1, wherein the insertion of the transmit time stamp into the reserved time stamp field is automatically performed for each test frame without intervention of the sending computers central processing unit(see paragraph [0081 – 0085]).

As to claim 10, Pruthi teaches the method of claim 1, wherein the receiving computer automatically attaches a receive time stamp corresponding to the synchronized time that the frame was received for each frame received (see paragraph [0081 – 0085]).

As to claim 11, Pruthi teaches the method of claim 1, wherein the receiving computer detects the tag of each test frame and attaches a receive time stamp corresponding to the synchronized time that the frame was received to only the test frames.

As to claim 12, Pruthi teaches the method of claim 1, wherein the creating step includes the step of creating complimentary time information in the reserved transmit and receive time stamp fields to enable the insertion of the synchronized transmit and receive time stamps upon transmit and receipt, respectively(see paragraph [0081 – 0085]).

As to claim 13, Pruthi teaches the method of claim 1, wherein the synchronized clocks have a resolution of between 10 and 100 nanoseconds (see paragraph [0081 – 0085]).

As to claim 14, Pruthi teaches a method for creating accurate time-stamped frames sent between computers via a network, comprising the steps of:

using a receiver to generate a universal coordinated time reference signal (see paragraph [0084 – 0085] Pruthi discloses the generation and reference signal packets);

synchronizing clocks associated with sending and receiving computers, but operating independently of operating system clocks of the sending or receiving computers, with the universal coordinated time reference signal by initializing the clocks with the received universal coordinated time reference signal and over time tracking and averaging the periodically received universal coordinated time reference signal and adjusting the clock to correspond to the universal coordinated time reference signal[0084 – 0085] Pruthi discloses the synchronization of host and the interface clocks);

creating a test frame including a tag having reserved fields for transmit and receive time stamps(see paragraph [0074 – 0078] and [0081 – 0082] Pruthi discloses the time stamped on a packet at two separate network monitors);

inserting a transmit time stamp into the reserved transmit time stamp field corresponding to the time on the synchronized clock of the sending computer at the instant the test frame is sent onto the network without intervention of the sending computer's central processing unit(see paragraph [0074 – 0078] Pruthi discloses each packet is stamped at the sending and receiving nodes); and

receiving the test frame having the transmit time stamp and inserting a receive time stamp into the reserved receive time stamp field corresponding to the time on the synchronized clock of the receiving computer when the test frame was received by the

receiving computer(see paragraph [0074 – 0078] Pruthi discloses each packet is stamped at the sending and receiving nodes).

As to claim 15, Pruthi teaches the method of claim 14, wherein the universal coordinated time signal is received via a global positioning system receiver in communication with either the sending or receiving computer(see paragraph [0081 – 0084]).

As to claim 16, Pruthi teaches the method of claim 15, wherein the clock and global positioning system receivers are electronically connected on a device which is attachable to an existing multi-master bus of either the sending or receiving computer(see paragraph [0081 – 0084]).

As to claim 17, Pruthi teaches the method of claim 16, wherein the device comprises a card interfacing with a multi-master bus of the receiving or sending computer (see paragraph [0081 – 0084] and [0143 – 0144]).

As to claim 18, Pruthi teaches the method of claim 14, wherein the synchronizing step includes the steps of altering the voltage applied to a voltage controlled crystal oscillator associated with the clock to maintain synchronization with the universal coordinated time signal (see paragraph [0081 – 0084]).

As to claim 19, Pruthi teaches the method of claim 14, wherein the receiving computer automatically attaches a receive time stamp corresponding to the synchronized time that the frame was received for each frame received (see paragraph [0081 – 0085]).

As to claim 20, Pruthi teaches the method of claim 14, wherein the receiving computer detects the tag of each test frame and attaches a receive time stamp corresponding to the synchronized time that the frame was received to only the test frames (see paragraph [0081 – 0085]).

As to claim 21, Pruthi teaches the method of claim 14, wherein the creating step includes the step of creating complimentary time information in the reserved transmit and receive time stamp fields to enable the insertion of the synchronized transmit and receive time stamps upon transmit and receipt, respectively (see paragraph [0081 – 0085]).

As to claim 22, Pruthi teaches the method of claim 14, wherein the synchronized clocks have a resolution of between 10 and 100 nanoseconds (see paragraph [0081 – 0085]).

As to claim 23, Pruthi teaches a method for creating accurate time-stamped frames sent between computers via a network, comprising the steps of:

using a global positioning receiver in communication with sending and receiving computers to generate a universal coordinated time reference signal(see paragraph [0064 – 0066]);

synchronizing clocks associated with the sending and receiving computers, but operating independently of operating system clocks of the sending or receiving computers, with the universal coordinated time reference signal by initializing the clocks with the received universal coordinated time reference signal and overtime tracking and averaging the periodically received universal coordinated time reference signal and

adjusting the clock to correspond to the universal coordinated time reference signal by altering the voltage applied to a voltage controlled crystal oscillator associated with the clock(see paragraph [0084 – 0085]);

creating a test frame including a tag having reserved fields for transmit and receive time stamps(see paragraph [0074 – 0078] and [0081 – 0082]);

creating complimentary time information in the reserved transmit and receive time stamp fields(see paragraph [0084 – 0085]);

replacing the complimentary time information in the transmit time stamp field with a transmit time stamp corresponding to the time on the synchronized clock of the sending computer at the instant the test frame is sent onto the network without intervention of the sending computer's central processing unit(see paragraph [0084 – 0085]); and

automatically attaching a receive time stamp corresponding to the time on the synchronized clock of the receiving computer when the frame was received by the receiving computer to every frame received by the receiving computer(see paragraph [0084 – 0085]).

As to claim 24, Pruthi teaches the method of claim 23, wherein the clock and global positioning system receivers are electronically connected on a device which is attachable to an existing multi-master bus of either the sending or receiving computer (see paragraph [0084 – 0085]).

As to claim 25, Pruthi teaches the method of claim 24, wherein the device comprises a card interfacing with a multi-master bus of the receiving or sending computer (see paragraph [0081 – 0084] and [01443 – 0134]).

As to claim 26, Pruthi teaches the method of claim 23, wherein the synchronized clocks have a resolution of between 10 and 100 nanoseconds (see paragraph [0081 – 0085]).

As to claim 27, Pruthi teaches a method for creating accurate time-stamped frames sent between computers via a network, comprising the steps of:

using a global positioning receiver in communication with sending and receiving computers to generate a universal coordinated time reference signal(see paragraph [0084 – 0085]);

synchronizing clocks associated with the sending and receiving computers, but operating independently of operating system clocks of the sending or receiving computers, with the universal coordinated time reference signal by initializing the clocks with the received universal coordinated time reference signal and over time tracking and averaging the periodically received universal coordinated time reference signal and adjusting the clock to correspond to the universal coordinated time reference signal by altering the voltage applied to a voltage controlled crystal oscillator associated with the clock(see paragraph [0084 – 0085]);

creating a test frame including a tag having reserved fields for transmit and receive time stamps(see paragraph [0074 – 0078] and [0081 – 0082]);

creating complimentary time information in the reserved transmit and receive time stamp fields(see paragraph [0084 – 0085])

replacing the complimentary time information in the transmit time stamp field with a transmit time stamp corresponding to the time on the synchronized clock of the sending computer at the instant the test frame is sent onto the network without intervention of the sending computer's central processing unit (see paragraph [0084 – 0085]); and

detecting the tag of each test frame received by the receiving computer and attaching a receive time stamp corresponding to the time on the synchronized clock of the receiving computer when the test frame was received by the receiving computer to the test frame (see paragraph [0084 – 0085]).

As to claim 28, Pruthi teaches the method of claim 27, wherein the clock and global positioning system receivers are electronically connected on a device which is attachable to an existing multi-master bus of either the sending or receiving computer (see paragraph [0081 – 0084] and [0143 – 0144]).

As to claim 29, Pruthi teaches the method of claim 28, wherein the device comprises a card interfacing with a multi-master bus of the receiving or sending computer(see paragraph [0081 – 0084] and [0143 – 0144]).

As to claim 30, Pruthi teaches the method of claim 28, wherein the synchronized clocks have a resolution of between 10 and 100 nanoseconds (see paragraph [0081 – 0085]).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure

.Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sargon N. Nano whose telephone number is (571) 272-4007. The examiner can normally be reached on 8 hour.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ario Etienne can be reached on (571) 272-4001. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sargon Nano
May 25, 2005

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